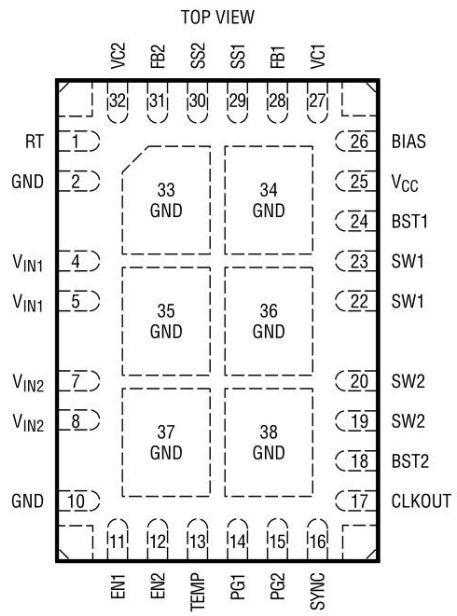
ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN1}, V_{IN2}, EN/UV1, EN/UV2, PG1, PG2.....42V
BIAS.....30V
FB1, FB2, SS1, SS2 .....4V
VC1, VC2.....3.5V
SYNC. 6V
Operating Junction Temperature Range (Note 2)
LT8650SE .....–40 to 125°C
LT8650SI .....–40 to 125°C
Storage Temperature Range .....–65 to 150°C
Maximum Reflow (Package Body)
Temperature.....260°C

Absolute Maximum Ratings will now show H Grade information.

PIN CONFIGURATION



LQFN PACKAGE
32-LEAD (6mm × 4mm × 0.94mm)
T_{JMAX} = 125°C, θ_{JA} = 23°C/W
EXPOSED PAD (PINS 33, 34, 35, 36, 37, 38) ARE GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

http://www.linear.com/product/LT8650S#orderinfo

PART NUMBER	PAD OR BALL FINISH	PART MARKING		PACKAGE** TYPE	MSL RATING	TEMPERATURE RANGE (SEE NOTE 2)
		DEVICE	FINISH CODE			
LT8650SEV#PBF	Au (RoHS)	8650SV	e4	LQFN (Laminate Package with QFN Footprint)	3	–40°C to 125°C
LT8650SIV#PBF						–40°C to 125°C

- Device temperature grade is indicated by a label on the shipping container.
- Pad or ball finish code is per IPC/JEDEC J-STD-609.
- Terminal Finish Part Marking: www.linear.com/leadfree
- Parts ending with PBF are RoHS and WEEE compliant.
- Recommended PCB Assembly and Manufacturing Procedures: www.linear.com/umodule/pcbassembly
- Package and Tray Drawings: www.linear.com/packaging

**The LT8650S package has the same dimensions as a standard 6mm × 4mm QFN package

Order Information updated to show H Grade. LT8650SHV#PBF and LT8650SHV#WPBF

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Input Voltage		●		2.6	3	V
V_{IN1} Quiescent Current in Shutdown	$V_{EN/UV1}$ = $V_{EN/UV2}$ = 0V, V_{SYNC} = 0V	 ●		1.7	4 ~~8~~ 10	µA µA
V_{IN1} + V_{CC} Quiescent Current in Sleep with Internal Compensation	$V_{EN/UV1}$ = $V_{EN/UV2}$ = 2V, V_{FB1} = V_{FB2} >0.8V, V_{VC1} = V_{VC2} = V_{CC}, V_{SYNC} = 0V	 ●		3.7	8 ~~16~~ 20	µA µA
V_{IN1} + V_{CC} Quiescent Current in Sleep with External Compensation	$V_{EN/UV1}$ = $V_{EN/UV2}$ = 2V, V_{FB1} = V_{FB2} >0.8V, V_{VC1} = V_{VC2} = Float, V_{SYNC} = 0V	 ●		90	120 140	µA µA

Rev A

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN1} + V_{CC} Quiescent Current when Active	$V_{EN/UV1}$ = $V_{EN/UV2}$ = 2V, V_{FB1} = V_{FB2} >0.8V, V_{VC1} = V_{VC2} = V_{CC}, V_{SYNC} = 3.4V	●		5	7	mA
V_{IN} Current in Regulation	V_{IN} = 12V, V_{OUT} = 3.3V, Output Load = 100µA, V_{VC1} = V_{VC2} = V_{CC}, V_{SYNC} = 0V V_{IN} = 12V, V_{OUT} = 3.3V, Output Load = 1mA, V_{VC1} = V_{VC2} = V_{CC}, V_{SYNC} = 0V			45 350	75 550	µA µA
Feedback Reference Voltage		 ●	0.794 0.790	0.800 0.800	0.806 0.810	V V
Feedback Voltage Line Regulation	V_{IN} = 4.0V to 36V			0.004	0.02	%/V
Feedback Pin Input Current	V_{FB} = 0.8V		–20		20	nA
Minimum On-Time	I_{LOAD} = 3A, SYNC = ~~3.4V~~ >= 2V	●		40	60	ns
Oscillator Frequency	R_T = 133k R_T = 35.7k R_T = 15k	● ● ●	270 ~~0.95~~ 0.94 1.85	300 1.0 2.00	330 ~~1.05~~ 1.06 2.15	kHz MHz MHz
Top Power NMOS Current Limit		●	10	12	14	A
Bottom Power NMOS Current Limit			6.5	8.5	10.5	A
SW Leakage Current	V_{IN} = 42V, V_{SW} = 0V,42V		–2		2	µA
EN/UV Pin Threshold	EN/UV Falling	●	0.7	0.74	0.78	V
EN/UV Pin Hysteresis				30		mV
EN/UV Pin Current	V_{EN}/UV = 2V		–20		20	nA
PG Upper Threshold Offset from V_{FB}	V_{FB} Falling	●	~~5.5~~ 5.4	~~7.5~~ 7.2	9	%
PG Lower Threshold Offset from V_{FB}	V_{FB} Rising	●	~~–0.5~~ -9.3	–7.5	~~–6~~ -5.7	%
PG Hysteresis				0.3		%
PG Leakage	V_{PG} = 12V		–40		40	nA
PG Pull-Down Resistance	V_{PG} = 0.1V	●		600	1200	Ohm
SYNC Threshold	SYNC DC and Clock Low Level Voltage SYNC Clock High Level Voltage SYNC DC High Level Voltage		0.4		 1.5 2.8	V V V
SYNC Pin Current	V_{SYNC} = 6V			120		µA
SS Source Current		●	1.0	2.0	3.0	µA
SS Pull-Down Resistance	Fault Condition, SS = 0.1V			200		Ω
Error Amplifier Transconductance	V_C = 1.25V			0.9		mS
VC Source Current	V_{FB} = 0.6V, V_{VC} = 1.25V			~~170~~ 185		µA
VC Sink Current	V_{FB} = 1.0V, V_{VC} = 1.25V			~~170~~ 185		µA
VC Pin to Switch Current Gain				9.6		A/V
TEMP Output Voltage	I_{TEMP} = 0µA, Temperature = 25°C I_{TEMP} = 0µA, Temperature = 125°C		~~100~~ ~~1100~~	250 1200	~~310~~ ~~1300~~	mV mV

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT8650SE is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization, and correlation with statistical process controls. The LT8650SI is guaranteed over the full –40°C to 125°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A in °C) and power dissipation (P_D, in Watts) according to the formula:

$T_J = T_A + (P_D \bullet \theta_{JA})$ where θ_{JA} (in °C/W) is the package thermal impedance.

Note 3: This IC includes overtemperature protection that is intended to protect the device during overload conditions. Junction temperature will exceed 150°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime